REMARKS/ARGUMENTS

Claims 1-29 are pending in this Application.

Claims 1-29 remain pending in the Application after entry of this Amendment. No new matter has been entered.

In the Office Action, claims 1-29 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,373,758 to Hughes et al. (hereinafter "Hughes").

Claim Rejections Under 35 U.S. C. § 102(b)

Applicants respectfully traverse the rejections to claims 1-29 and request reconsideration and withdrawal of the rejections under 35 U.S.C. § 102(b) based on Hughes.

Applicants respectfully note that to anticipate a pending claim, a prior art reference must provide, either expressly or inherently, each and every limitation of the pending claim. (M.P.E.P. § 2131).

The Office Action alleges that Hughes teaches or suggests all of the claim limitations of claims 1-29. However, based on the arguments presented below, Applicants respectfully submit that Hughes fails to teach or suggest at least one of the claim limitation recited in each of claims 1-29.

Claim 1

Claim 1 recites a method for repairing defective memory elements using self-test circuitry in a memory having a plurality of memory elements including a first memory element and a second memory element. The method includes:

counting fails in the first memory element with an on-chip logic counter;

counting fails in the second memory element with the on-chip logic counter;

comparing the number of fails in the first memory element to the number of fails in the second memory element;

determining the one of the first memory element and the second memory element having the most fails; and

allocating a redundant memory element to replace the one of the first memory element and the second memory element having the most fails.

Applicants respectfully submit that Hughes fails to teach or suggest one or more of the claim limitations recited in claim 1. For example, the Office Action alleges that Hughes discloses the features recited in claim 1 of "comparing the number of fails in the first memory element to the number of fails in the second memory element" and "determining the one of the first memory element and the second memory element having the most fails" in FIG. 5; Col. 10, line 49 to Col. 11, line 39. Applicants respectfully disagree.

As recited in claim 1, fails in a first memory element and fails in a second memory element are counted with an on-chip logic counter. The number of fails in the first memory element is compared as recited in claim 1 to the number of fails in the second memory element. The one of the first memory element and the second memory element recited in claim 1 is then determined as having the most fails.

Hughes discloses that if a memory cell's stored value does not match the expected data, the integer value stored in counter 507 is incremented to count either the total number of fails or a saturation value. (Hughes: Col. 11, lines 5-6). Hughes further discloses that testing in this manner is completed for each cell in each column and the values representing total failures or saturation values are associated with each column of each memory array. (Hughes: Col. 11, lines 11-13). Thus, in Hughes, columns are identified which have failed BIST by having at least a predetermined number of failed cells. Redundant columns are then used to replace those columns. (Hughes: Col. 11, lines 14-16; Emphasis added).

Hughes fails to teach or suggest that the number of fails in a first memory element is compared as recited in claim 1 to the number of fails in a second memory element, and that the one of the first memory element and the second memory element is determined as recited in claim 1 having the most fails. As discussed above, Hughes simply compares a predetermined number of fails (e.g., one more than the number of available replacements or a saturation value) to the number of fails registered for each column. This process of checking the number of fails against a predetermined number of fails is substantially different from comparing the number of fails in a first memory element to the number of fails in a second memory element as recited in

claim 1. Accordingly, Applicants respectfully submit that Hughes fails to teach or suggest that the number of fails for a first that the number of fails in a first memory element is compared as recited in claim 1 to the number of fails in a second memory element.

Moreover, Hughes fails to teach or suggest that the one of the first memory element and the second memory element having the most fails is determined as recited in claim 1 during the iterative process of replacement in Hughes. (Emphasis added). Hughes merely discloses that one or more columns/rows are replaced if the number of fails exceeds a predetermined threshold or meets the saturation value. (Hughes: Col. 10, lines 29-48). Hughes fails to disclose a determination between a first memory element and a second memory element for the one having the most fails as recited in claim 1.

Furthermore, Hughes fails to teach or suggest allocating a redundant memory element to replace the one of the first memory element and the second memory element having the most fails as recited in claim 1. As discussed above, Hughes iterates through one or more test cycles and replaces each column/row that has errors that exceed a predetermined threshold or meet a saturation value. Replacing each column/row that has errors that exceed a predetermined threshold or saturation value as in Hughes is substantially different from allocating a redundant memory element as the replacement for a given memory element determined as having the most fails as recited in claim 1. (Emphasis added).

Accordingly, Applicants respectfully submit that Hughes fails to teach or suggest each and every claim limitation recited in claim 1. Thus, Applicants respectfully submit that claim 1 is allowable over the cited references.

Claim 16

Applicants respectfully submit that independent claim 16 is allowable for at least a similar rationale as discussed above for the allowability of claim 1, and others. For example, claim 16 recites "a compare circuit that compares the number of fails in each of the memory elements and records the memory element having the most fails."

The Office Action again points to FIG. 5; Col. 10, line 49 to Col. 11, line 39 of Hughes as allegedly disclosing the compare circuitry recited in claim 16. Applicants respectfully

disagree. The Office Action has failed to identify any structure in the figures of Hughes that discloses compare circuitry that compares the number of fails in each of the memory elements and records the memory element having the most fails as recited in claim 16. Moreover, as discussed above, Col. 10, line 49 to Col. 11, line 39 of Hughes previously point to in the Office Action simply disclose that the total number of fails of an individual column/row is compared to a predetermined threshold or saturation value. Hughes fails to disclose a comparison between the number of fails in each of the memory elements as recited in claim 16.

Moreover, Hughes merely discloses that the total number of fails for a column is counted. Simply counting the total number of fails for each column as in Hughes fails to teach or suggest compare circuit that records the memory element having the most fails as recited in claim 16.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 925-472-5000.

Respectfully submitted,

/Sean F. Parmenter/
Sean F. Parmenter
Reg. No. 53,437

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: 925-472-5000
Fax: 415-576-0300
SFP:pas
61094043 v1